

English Translation of JP61-80226**(19) Japanese Patent Office (JP)****(11) Laid-open No. : Sho 61-80226****(43) Laid open Date : April 23, 1986****5 (12) Patent Laid-open Official Gazette (A)****Request for Examination: not made****The Number of Inventions: 1 (14 pages in total)****(54) Title of the Invention: Active Matrix Driving Device****10 (21) Application No. : Sho 59-201529****(22) Application Date : September 28, 1984****(72) Inventor : Osamu ICHIKAWA****c/o TOSHIBA Corporate Research & Development Center****1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki-shi****15 (72) Inventor : Toyoki HIGUCHI****c/o TOSHIBA Corporate Research & Development Center****1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki-shi****(71) Applicant : TOSHIBA CORPORATION****72, Horikawa-cho, Saiwai-ku, Kawasaki-shi****20****25**

Specification

1. Title of the Invention

ACTIVE MATRIX DRIVING DEVICE

5 2. Scope of Claim

[Claim 1]

An active matrix driving device characterized by comprising:

an active matrix part in which switching elements and electrode interconnections for driving the switching elements are formed in a matrix form;

10 a plurality of switching elements which are provided correspondingly to each interconnection extended from the active matrix part, selectively drive each of said interconnections extended by two-type signals, and are block-segmented by the same number;

first electrode interconnections which are provided at each of said plural block sections, and supply one of said two-type signals to all of said switching elements of each of said block
15 sections; and

second electrode interconnections which are provided correspondingly to the number of the switching elements of said each block section, and supply the other signals of said two-type signals to each one of the switching elements of said each block section.

[Claim 2]

20 An active matrix driving device as set forth in claim 1 characterized in that switching elements of said active matrix part are comprised of TFTs (Thin Film Transistor).

[Claim 3]

An active matrix driving device as set forth in claim 1 characterized in that electrode interconnections of said active matrix part are comprised of address interconnections and data
25 interconnections.

[Claim 4]

An active matrix driving device as set forth in claim 1 characterized in that each interconnection extended from said active matrix part is the extension of the electrode interconnections of said active matrix part.

[Claim 5]

An active matrix driving device as set forth in claim 1 characterized in that each interconnection extended from said active matrix part is electrically connected to electrode interconnections of said active matrix part by elastomer or a wire bonding method.

5 [Claim 6]

An active matrix driving device as set forth in claim 1 characterized in that a plurality of switching elements which selectively drive each of said interconnections extended by said two-type signals are comprised of TFTs (Thin Film Transistor).

[Claim 7]

10 An active matrix driving device as set forth in claim 1 characterized in that a plurality of switching elements which selectively drive each of said interconnections extended by said two-type signals are comprised of TMG (Transmission Gate) chips.

[Claim 8]

15 An active matrix driving device as set forth in claim 7 characterized in that said blocks are comprised of TMG (Transmission Gate) ICs.

[Claim 9]

An active matrix driving device as set forth in claim 3 characterized in that first electrode interconnections for driving said address interconnections are selected by ICs for address selection.

20 [Claim 10]

An active matrix driving device as set forth in claim 3 characterized in that second electrode interconnections for driving said address interconnections are selected by ICs for an address driver.

[Claim 11]

25 An active matrix driving device as set forth in claim 3 characterized in that first electrode interconnections for driving said data interconnections are selected by ICs for data selection.

[Claim 12]

An active matrix driving device as set forth in claim 3 characterized in that second electrode interconnections for driving said data interconnections are selected by ICs for data

latch.

3. Detailed Description of the Invention

[Technical Field to which the Invention belongs]

The present invention relates to a driving device for a display device in which switching
5 elements are arranged in a matrix form, and more particularly to an active matrix driving device
which has a peripheral driving circuit.

[Technical Background of the Invention and its problems]

Display devices such as electroluminescence, a light emitting diode, plasma, a
fluorescence display part and a liquid crystal can be made thin at their display parts and a
10 growing demand has been made for them to be used as terminal display devices of a measuring
apparatus, a business machine and a computer or the like or a special display device. Of these
display devices, greater attention has been paid to the liquid crystal display device in view of its
low electric power consumption and cost.

Recently, to further improve the performance of the liquid crystal display device,
15 switching elements using thin film transistors formed in a matrix array have been developed.
By this method, image data is stored in each dot of a switching transistor matrix provided on a
substrate and a change of a liquid crystal layer positioned correspondingly to each dot of the
matrix array is held for a predetermined time, thereby a desired image is displayed.

Accordingly, a liquid crystal display device with a switching transistor matrix array
20 performs an almost full-time image display and a high-quality of reproduction image can be
obtained.

Meanwhile, as a material for a switching transistor, such as SI, CdSe, Te, CdS or the like
in a crystalline, polycrystalline, or amorphous state are used. Above all, the thin film technique
for a polycrystalline semiconductor and an amorphous semiconductor can achieve a low
25 temperature process, thereby can form active matrix elements of switching transistors even on a
substrate such as a glass substrate which needs to be treated in a relatively low temperature. It
is, therefore, possible to produce a large area display device at low cost for practical use.

Conventionally, such an active matrix array substrate was constituted of just a display
part, and it was connected to a driving circuit part provided at an external part by a wire bonding

method or the like so as to display images on a matrix array substrate as the display part.

FIGs. 15(a) and 15(b) show a general connecting method of a substrate display part and a driving circuit substrate in a transmission active matrix liquid crystal display device.

A substrate display part 2 is constituted of a substrate on which a thin transistor array is
5 configured, a substrate formed of a transparent power source on the whole surface facing to the
former substrate, and a liquid crystal layer sandwiched between the two substrates. Meanwhile,
a peripheral driving circuit 4 is constituted of a PC board having a window in the center to
embed the substrate display part 2 and a plurality of ICs 6 peripherally. For holding the
substrate display part 2, a transparent holding substrate 8 equipped on the reverse side of the
10 peripheral driving circuit substrate 4 is used, and electrode terminals provided on the periphery
of the substrate display part 2 and on the periphery of the window of the driving circuit substrate
4 are mutually connected by a bonding wire 10. Although an IC is used as a chip in this
built-up structure, it may also be structured with a DIPIC by making use of the characteristics of
a PC board. Further, it is possible to adopt a simple structure without window-opening in the
15 central part of the driving circuit substrate nor a holding substrate if a transparent glass substrate
is used in place of a PC board.

However, when an active matrix display device of a large screen with high-definition is
structured, the number of terminals provided on a periphery part on a substrate display part
increases. Meanwhile, bonding pads of the ICs of the present condition are provided at 4 sides
20 around a chip, and the spacing is 100 to 150 μm . For this reason, turnaround interconnections
are required for peripheral interconnections of the part loaded with IC chips even if a terminal
pitch of the substrate display part is 150 to 200 μm . Therefore, a measure of having multilevel
interconnections is taken. The multilevel interconnections on the periphery of the part loaded
with these IC chips have been made mostly through a different process from that of the structure
25 of the thin film transistor matrix array part. This led to a low manufacturing yield of the matrix
array substrate display part, and further to notable waning productivity as a whole display device
because of the defects generating during the manufacture of the IC chips.

FIG 16 shows a conceptual configuration view of these driving circuits. First, an input
signal 12 such as image data, a vertical signal, a horizontal signal, a clock signal or the like from

external devices are inputted to a control circuit 14. A clock signal 16 and image data 18a, 18b generated on the control circuit 14 are inputted to image data processing circuits (one line memories) 20a, 20b and image scanning signals 22a, 22b are inputted to line scanning circuits 24a, 24b. Then, signals from the line scanning circuits 24a, 24b and the image data processing
5 circuits 20a, 20b are inputted to a display part 2 and images are displayed on it. A thin film transistor formed inside the display part 2 as a display element array is slow at its response speed, so image data for one line is stored with ICs which can operate relatively at high speed in the image data processing circuits 20a, 20b, and in the line scanning circuits 24a, 24b, what is called a line sequential scanning which can scan at relatively low speed is adopted. Meanwhile, by
10 this method, a scanning process of jumping over line by line is taken: uneven numbers are scanned first as G1, G3,...Gn on the line scanning circuit 24a followed by a scanning of even numbers as G2, G4, G6,...Gn+1 as a television scanning of NTSC system, in consideration of insufficient writing of data corresponding to one line scanning (applying a gate voltage to TFT) when the line scanning increases in number. Further, as a means to moderate a pitch of a
15 terminal corresponding to an image pitch, even and uneven numbers are similarly divided at the image data processing circuits 20a, 20b.

In case of configuring ICs of an existing dual in-line package type or the like on a PC board for these driving circuits, the problem will be solved by manipulating the connection of the ICs to the substrate display part corresponding to the line scanning of even and uneven
20 numbers. However, when IC chips were loaded on the substrate display part as described above so as to miniaturize the whole display device, two types of ICs, each of which has the same function, and output terminals of which were inverted in position were needed for an image data processing circuit and for a line scanning circuit, thereby led to the low productivity of ICs and efficiency of its assembling. Meanwhile, a LSI of a CMOS or the like is used for a
25 peripheral driving circuit in itself for lowering the electric power consumption. For this, 20 to 50 IC chips are needed, resulting in high cost of assembly and IC chips per se as well as the increasing electric power consumption.

Recently, as a means to handle the foregoing problems, considered is what is called an integral display device with a peripheral driving circuit part, formed of a shift register integrally

on the periphery of the substrate display part. However, when a shift register is formed with a conventional thin film transistor technique, problems concerning processing precision and a manufacturing process occur because an interconnection pattern of the shift register becomes minute as compared to the display part, and further a response speed becomes late because many distorted signal waveforms occur when a driving circuit of a general MOS structure is configured since the film is thin. Incidentally, the whole driving circuit substrate for a display device becomes defective unless an yield of the shift register is 100%. As shown in a patent laid-open official gazette sho59-58480, in the case where a driving circuit is improved at its speed using clock signals of more than 4 phases or at its yield by providing dummy cells on a shift register, an interconnection pattern becomes highly minute leading to a problem as to the processing precision. Further, a problem of an increase in circuit scale of a peripheral driving part occurs.

Note that, on what is called a simple matrix liquid crystal display device comprising straight row electrodes and column electrodes, driving circuits can be reduced by multiplexing selective scanning operations of the row electrodes according to a patent laid-open official gazette sho59-48738. This method, however, has a problem: in case of 16 x 16 (256) pixels for example, the number of connecting points between a display part and a driving circuit part becomes 256 in column and 32 in row, and after all, the number of connecting points cannot be reduced to a large degree.

Meanwhile, considered is a case where wire connections as memory ICs such as RAMs, data selector ICs and recorder ICs or the like are used. However in that case, a driving circuit which sends stable electrical signals for an active matrix is needed, and a driving circuit which can send a large amount of electrical signals to switching elements of an active matrix part and has a high-speed selective drive operation is also needed.

[Purpose of the Invention]

The purpose of the present invention is to provide a driving device for a display device which can drive a large number of matrix array terminals of a display part with a small number of ICs for driving without lowering a manufacturing yield of a matrix array of the display part concerning a case of combining the above-mentioned display part of the active matrix array and

the peripheral driving circuit which drives the display part.

[Abstract of the Invention]

The present invention is to obtain an active matrix driving device comprising:

an active matrix part in which switching elements and electrode interconnections for

5 driving the switching elements are provided in a matrix form,

a plurality of switching elements which are provided correspondingly to each interconnection extended from the active matrix part and selectively drive each interconnection extended by two-type signals,

10 a plurality of block sections where the plurality of switching elements are segmented by the same plural number of the switching elements,

first electrode interconnections which are provided at each of the plural block sections and supply one of two-type signals to every switching element of each block section, and

15 second electrode interconnections which are provided correspondingly to the number of the switching elements of each block section and supply the other signals of the two-type signals to one switching element of every block section.

[Effect of the Invention]

By disposing switching element groups which have the foregoing functions on the periphery of an active matrix display element array on a driving circuit substrate for a display device, the number of integrated circuits which form electrical signals for giving to matrix
20 terminals can be reduced even if there are a large number of matrix terminals. Accordingly, connecting points by a bonding method or the like can be reduced drastically as well as the reduced electric power consumption for driving.

Meanwhile, a high yield can be obtained because rougher patterns than those of the switching elements of the display part matrix array may be used. Further, an active matrix
25 driving circuit substrate which has highly improved productivity and larger flexibility on packaging design can be obtained because an assembly area of the peripheral driving circuit can be reduced as compared to an area of the display part.

Incidentally, a high-speed selective drive operation of an active matrix part can be achieved because the selective drive operation of the peripheral driving circuit according to the

present invention can be performed at every switching element group (blocks).

[Embodiments of the Invention]

Embodiments of the present invention are explained below with reference to FIGs. 1 to 14. First, FIG. 1 is a plan view of a driving circuit substrate for a display device using an embodiment of the present invention. FIGs. 2 (a), 2(b) and 2(c) are respectively an equivalent circuit diagram, a plan view and its sectional view of a display part which occupies a central region of a driving circuit substrate for a display device as shown in FIG. 1. FIGs. 3 (a) and 3(b) are a plan view and its sectional view of a peripheral driving circuit part which occupies a peripheral region of a driving circuit substrate for a display device. A driving circuit substrate for a display device as shown in this embodiment is formed of address electrodes(32), (32a), (32b),...(32w) for a display part, peripheral source interconnection terminal parts (34a),...(34h), (34i), ...(34s) and peripheral gate interconnections(36a), (36b),...(36h) for a peripheral driving circuit part on a transparent glass substrate(30) altogether, further formed of a silicon oxide film(40) which has through-hole parts(38). Semiconductor thin films(42a), (42b),...(42g) of island-shaped patterns formed of amorphous silicon, for example, are provided respectively corresponding to the address electrodes(32a), (32b),...(32w) formed regions on the silicon oxide film(40) of a substrate display part, and also corresponding to the peripheral gate interconnections(36a), (36b),...(36h) formed regions on the silicon oxide film(40) of a substrate peripheral part. Data electrodes(44), (44a),...(44w) are formed connecting to one end of the semiconductor thin film(42) of the substrate display part, and a drain electrode(46) to the other end so as to form switching elements. Peripheral source electrodes(50a),...(50g) are formed connecting to one ends of semiconductor thin films(42a),....(42g) of the peripheral part of the substrate, and peripheral drain electrodes (52a),....(52g) to the other ends. Further, portions of the peripheral source electrodes(50a),....(50g) are connected to the peripheral source interconnection terminal parts(34a), (34b),...(34h) through the through-hole parts(38), and portions of the peripheral drain electrodes(52a),...(52g) are connected to the address electrodes(32a),....(32w) of the display part through the through-hole parts(38). When such a driving circuit substrate for a display device is used for a liquid crystal display device, a pixel electrode(53) comprised of, for example, ITO(Indium Thin Oxide) has only to be formed

connecting to the drain electrode(46) as shown in FIG 2(b), and further a transparent facing substrate(58) formed of a transparent conductive film(56) comprised of, for example, ITO over its inner side should be provided through a liquid crystal layer(54) on the display part region of the transparent glass substrate(30).

5 Next, explained is a manufacturing method of the above driving circuit substrate for a display device. First, a Mo film of 2000Å is accreted on the transparent glass substrate(30) of approximately 2mm in thickness and the address electrodes(32a), (32b),...(32w), the peripheral source interconnection terminal parts(34a), (34b),...(34h) and the peripheral gate interconnections(36a), (36b),...(36h) which are to become first layer patterns are formed by a
10 PEP(Photo Engraving Process) technique. Next, the silicon oxide film(40) is accreted on it by 2000Å using a CVD method, and through-hole parts(38) are formed on the desired positions thereof. Then, and amorphous silicon is accreted on it by approximately 3000Å using the CVD (Chemical Vapour Deposition) method and the semiconductor thin films(42a), (42b),...(42g) of island-shaped patterns are formed by the PEP technique.

15 Then, a transparent conductive layer comprised of ITO of 3000 Å is accreted and the pixel electrode(53) is formed by patterning using the PEP technique. Subsequently, Mo of approximately 500Å and aluminum of approximately 1µm are laminated by sputtering or deposition and the drain electrode(46) inside the display part, the data electrodes(44), (44a),(44b),...(44w), the peripheral drain electrodes(52),(52a),...(52g), the peripheral source
20 electrodes(50), (50a), (50b), ...(50g) and an IC connecting point for driving which are to become second layer patterns are formed. Thus, a TFT(62) inside the display part and peripheral switching transistor groups(64a), (64b),...(64h) are formed.

Although as shown in FIGs. 1 to 3, the address electrodes(32), (32a), (32b)...(32w) which run on the TFT(62) inside the display part are a first layer, and through-hole parts(38)
25 should be provided by thirling the silicon oxide film(40) as an insulating film to connect the peripheral drain electrodes(52), (52a), (52b),...(52g) as a second layer, no through-hole parts are required for the connection between a peripheral drain electrode(66) and the data electrodes(44), (44a), (44b)...(44w) which run on the TFT(62) inside the display part.

On ends of the gate interconnection parts(36a), (36b),...(36h) and the peripheral source

interconnection terminal parts(34a), (34b),...(34h),(34l),...(34s) which connect source electrode parts of the peripheral switching transistor groups(64a), (64b), (64c),...(64h) in common, the driving IC interconnection part (60) is provided so as to be connected to a driving circuit part(not shown in FIGs.) provided outside of the driving circuit substrate(30) by a wire bonding method or a pressure welding with a conductive rubber or the like, thus given desired electrical signals.

On the driving circuit substrate for a display device constructed as the above, the address electrodes(32a),...(32w) of the display part are selected by turning ON the peripheral transistor groups(64a),...(64d) by the gate electrode interconnections(36a),...(36d) and the peripheral source interconnection terminal parts(34a),...(34h) of the peripheral driving circuit part. Similarly, the data electrodes(44a), (44w) of the display part are selected by turning ON the peripheral transistor groups (64e),...(64h) by the gate electrode interconnections(36e),...(36h) and the peripheral source electrode terminal parts(34l),...(34s) of the peripheral driving circuit part. When the driving circuit substrate is used for the liquid crystal display device as shown in FIG 2, the TFT(62) inside the display part is further selected by selecting the address electrodes(32a),...(32w) of the display part and the data electrodes(44a),...(44w) as the above, and thus pixel electrodes(48) corresponding to each TFT(62) are applied voltages to drive a liquid crystal layer(54). Thus, optional display images are displayed by selectively combining the pixel electrodes(48) arranged in a matrix form.

Note that, in the foregoing embodiment, driving circuit parts such as a selector or a driver are not provided on the peripheral driving circuit part, ICs for data selection(70), ICs for data latch(72), ICs for an address driver(74) and ICs for address selection(72) can be set on the peripheral driving circuit part as shown in FIG 4.

That is to say, according to the present invention, only an IC for selection and an IC for latch or an IC for a driver and an IC for selection have to be provided correspondingly to each side of an active matrix part, thus a circuit scale can be reduced to a large degree without having a latch function or an amplifying function correspondingly to each data or each address line as the case where a conventional shift register is used.

Meanwhile, the present invention has an advantage of being able to drastically reduce the

number of interconnections of an active matrix driving circuit substrate with external devices which are to be image information sources.

Incidentally, as to a driving circuit substrate for a display device according to the present invention, a display part and a peripheral driving circuit part can be separately manufactured, and each terminal of a display part and a peripheral driving circuit part can be connected by elastomer or a wire bonding method. When the display part and the peripheral driving circuit part are manufactured in different processes like this, switching elements on the peripheral driving circuit part may not necessarily be a TFT as the above embodiment. For example, as shown in FIG 6, the switching elements may be constituted of TMG (Transmission Gate) chips(80) as shown in FIGs. 5(a), 5(b) and 5(c). Further, assembly can be omitted if ICs(82) which are constituted of a larger number of TMG elements are used as shown in FIG 7.

Next, explained are operations of the present invention with reference to FIGs. 8 to 14. FIGs. 8(a) and 8(b) show a plan view and its equivalent circuit view of a peripheral driving circuit part constituted of peripheral switching transistor groups T_1, T_2, T_3, T_4 . The FIGs. 8(a) and 8(b) show a peripheral driving circuit in the case where the number of drain electrodes of one side for a display part are 16, wherein, the switching transistor groups T_1, T_2, T_3, T_4 which have common gates are provided and drain electrodes D_1 to D_{16} may be selected by selecting source electrodes S_1 to S_4 and common gate electrodes G_1 to G_4 .

FIGs. 9(a) and 9(b) show signal generating circuits to source electrode interconnections S_1, S_2, S_3, S_4 and gate electrode interconnections G_1, G_2, G_3, G_4 . In FIG 9(a), an FF counter(80) conducts a binary count by a clock signal CK which has predetermined width of time. The counter(80) sends upper 2 bits of binary signals(82) and a first decoder(84) outputs its decoder signals S_1, S_2, S_3, S_4 . Meanwhile, lower bits of binary signals(86) in the counter(80) are given to a second decoder(88) to generate its decoder signals G_1, G_2, G_3, G_4 . Incidentally, in FIG 9(b), two pairs of shift registers are used in place of the counter and the decoders in FIG 9(a). First, initial data D is inputted to a first shift register (90) and appears on S_1 in synchronism with a clock signal CK. Then, a second clock signal CK is excited by omitting the initial data D so as to switch an output of the first shift register(90) to S_3, S_4 . As to output signals G_1, G_2, G_3, G_4 of a second shift register(92), G_1 is On in an initial condition. The output of the second shift register(92) is

switched to G_2 by combination of a carry signal CY of the first shift register(90) and the clock signal CK. The input data signal D to the first shift register(90) generates at every predetermined period, and in this case, it generates at every output of the S_4 . Thus, in FIGs. 9(a) and 9(b), the circuit are constituted of output signals G_1, G_2, G_3, G_4 switching at every circuit scanning S_1, S_2, S_3, S_4 .

Fig. 10 is a time chart of the signals from the driving circuit of FIG. 9(a) or 9(b) and the output signals of the drain electrode interconnections D_1, D_2, \dots, D_{16} of the peripheral switching transistor groups T_1, T_2, T_3, T_4 . As shown in FIG. 6, the source electrode interconnections S_1, S_2, S_3, S_4 are sequentially inputted ON signals when each of the gate electrode interconnections G_1, G_2, G_3, G_4 are ON for a predetermined period. If the S_1, S_2, S_3, S_4 are sequentially scanned every time the gate electrode interconnections G_1, G_2, G_3, G_4 are switched, the drain electrode interconnections D_1, D_2, \dots, D_{16} of the switching transistor groups T_1, T_2, T_3, T_4 output signals sequentially, thus they are available as scanning signals of the address electrodes of the TFTs in the display part.

Meanwhile, for a data signal to a TFT inside the display part, a parallel signal is more favorable than a serial signal. FIGs. 11 and 12 respectively show an image data processing circuit and its time chart using peripheral switching transistor groups relating to the present invention. First, an analogue image signal AD in synchronism with a clock signal CK is stored in a predetermined part of a sample/hold (86) according to an output signal(96) of a shift register(94). Analogue image information(100) stored in the sample/hold(86) is amplified by an analogue driver(102) and generates respective output signals S_1, S_2, S_3, S_4 . Meanwhile, output modes of the binary signal(96) are switched to a counter(98) every time ordinary writing to the shift register(94) has finished, and decode output signals G_1, G_2, G_3, G_4 are switched by a decoder(104) of the last stage. By this method, the output signals D_1, D_2, \dots, D_{16} from the peripheral switching transistor groups T_1, T_2, T_3, T_4 are simultaneously outputted by four with each own amount of analogue information by combining analogue image information signals S_1, S_2, S_3, S_4 and decode signals G_1, G_2, G_3, G_4 .

As above, an active matrix image display scanning can be conducted by concurrently working a function of switching transistor groups of an image data side and a function of switching transistor groups of an address scanning side. Namely, as shown in FIG. 13, by letting a parallel

output of an image data side make a circuit within a decode output period T of an address scanning side, a displaying operation, the line sequential scanning style of which is transformed can be conducted.

FIG 14 shows a driving circuit substrate which has IC chips on board by devising an IC
5 connecting point for driving(60) shown in FIG. 1. Image data and scanning signals of external devices are received from I/O terminal parts(92) and an address scanning and an image data processing are conducted at ICs 90,90a,...90h which operate desirably. Thus, an address scanning is operated by switches. A display scanning is conducted by switching transistor groups(94) and switching transistor groups(96) which output image data sequentially. Accordingly, image is
10 displayed at a display part(98).

Note that, in the embodiments of the present invention, peripheral switching transistor groups are provided at an image data side as well as an address scanning side to simplify operations with peripheral driving ICs. Although there are cases where image data writing for a predetermined period is insufficient when storage capacitance is added to pixel cells inside a display
15 part or when amorphous silicon is used as a material for a semiconductor thin film, in these cases, a conventional wire connecting method may be used together without providing switching transistor groups at an image data side.

Meanwhile, although in the embodiments, explained are switching transistor groups as 4, it is, needless to say, effective to apply the present invention to a driving circuit substrate for a display
20 device which needs a considerably large number of terminals for the intended original purpose. Particularly, it is effective when the number of addresses is 500 to 1000, and the number of a data side is 500 to 2000.

4. Brief Description of the Drawings

FIG 1 is a view showing an embodiment of the present invention, FIGs. 2 to 14 are views to
25 explain the other embodiments of the present invention and FIGs. 15 and 16 are views showing conventional embodiments.

30: Transparent glass substrate, 32, 32a, 32b,...32w: Address electrode interconnections for a display part, 34a, ...34h, 34l,...34s: Peripheral source interconnection terminal parts, 36a,

36b,...36h: Peripheral gate interconnections, 38: Through-hole part, 40: Silicon oxide film,
42,42a,...42g: Semiconductor thin films, 44, 44a,...44w: Data electrodes, 46: Drain electrode,
50a, 50b,...50g: Peripheral source electrodes, 52a, 52b,...52g: Peripheral drain electrodes,
53: Pixel electrode, 54: Liquid crystal layer, 56: Transparent conductive film, 58: Facing
5 substrate, 60: IC connecting point for driving, 62: TFT, 64a, 64b,...64h: Peripheral
switching transistor groups, 66: Peripheral drain electrode, 70: IC for data selection, 72: IC
for data latch, 74: IC for an address driver, 76: IC for address selection